ABSTRACT OF THE DISCLOSURE

A semiconductor memory device that reduces the probability of the penalties of wirings arising. An address input circuit receives an address signal input. A drive circuit drives a memory array in compliance with the address signal. A signal line connects the address input circuit and the drive circuit. A redundant circuit is located near the drive circuit and substitutes other lines including a redundant line for a defective line in the memory array. A defective line information store circuit stores information showing the defective line. A supply circuit supplies information stored in the defective line information store circuit to the redundant circuit via the signal line. This structure enables to transmit an address signal and information regarding a defective line by a common signal line and to reduce the number of wirings and the probability of the penalties of wirings arising.